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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/671,150	09/28/2000	Wataru Domon	017344/0312	8461

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EXAMINER	
TRAN, PHUC H	

ART UNIT	PAPER NUMBER
2666	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/671,150	DOMON ET AL.	
	Examiner	Art Unit	
	PHUC H TRAN	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,18,19,21,25 and 26* is/are rejected.

7)☒ Claim(s) *5-17,20 and 22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 18-19, and 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito (U.S. Patent No. 6509988 B1)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

- With respect to claims 1, 18 and 19, Saito discloses the claimed invention:

a speed converter for converting the speed of packets (physical layer interface having a speed setting circuit for setting the top speed of an IEEE serial bus node col. 1 lines 51-53) transmitted between first and second communication nodes respectively attached to first and second IEEE-1394 serial buses, comprising:

a first transceiver node for receiving an inbound first packet at a first speed from the first bus and transmitting an inbound second packet as an outbound second packet at the first speed to

the first bus; a second transceiver node for transmitting the inbound first packet as an outbound first packet at a second speed to the second bus and receiving the inbound second packet at the second speed from the second bus (port transceivers 10 and 11 operating with a target node over respective serial buses, are connected to a data link which performs data format conversion between the data strobe signals to and from port transceivers. A first speed setting circuit located in a first port transceiver of the plurality of port transceiver and a second speed setting circuit located in a second port transceiver col. 2 lines 13-18 and col. 3 lines 7-15);

header translation circuitry for translating destination identifier of the inbound first packet to destination identifier of the outbound first packet according to a mapped relationship between the first transceiver node and the second communication node, and translating destination identifier of the inbound second packet to destination identifier of the outbound second packet (a compare-and- select circuit for comparing the operating speed set by the first speed setting circuit with the operating speed set by the second speed setting circuit col. 2 lines 19-21).

- With respect to claim 2, Saito discloses a first physical layer processor connected to the first bus;

a first link layer processor connected to the first physical layer processor (physical layer interface of an IEEE-1394 serial bus node comprising a plurality of port transceivers connected to a controller performing data conversions between the link layer and transceivers col. 2 lines 4-13);

and first speed setting means for setting a value representative of the first speed into the first link layer processor (first speed setting circuit located in a first transceiver of a plurality of

port transceivers col. 2 lines 13-15), wherein the second transceiver node comprises: a second physical layer processor connected to the second bus; a second link layer processor connected to the second physical layer processor (physical layer interface of an IEEE-1394 serial bus node comprising a plurality of port transceivers connected to a controller performing data conversions between the link layer and transceivers col. 2 lines 4-13);

and second speed setting means for setting a value representative of the second speed into the second link layer processor (a second speed setting circuit located in a second port transceiver of the plurality of port transceivers col. 2 lines 17-19), wherein the header translation circuitry comprises:

a memory for storing identifiers for mapping the first transceiver node to the second communication node (a register for storing operating parameters col. 1 lines 63-64);

and control circuitry connected to the first and second link layer processors for receiving a packet therefrom and rewriting destination identifier of the packet according to the identifiers stored in the memory when a transaction is initiated from the first bus(a controller connected to the link layer and port transceivers arranged to read the stored speed value from the register, receive a speed value form another node and begin packet transmission col. 2 lines 1-26)

-With respect to claim 3, Saito teaches wherein the memory further stores identifiers for mapping the second transceiver node to the first communication node (a register for storing operating parameters of the controller under the control of the link layer col. 3 lines 41-43), and wherein the control circuitry receives a packet from the second transceiver node and rewrites destination identifier of the packet according to the identifiers stored in the memory when a

transaction is initiated from the second bus (controller arranged to read the stored speed value from the register, performs arbitration between communicating nodes col. 3 lines 912).

- With respect to claims 25-26, Saito teaches wherein the first speed is different from the second speed (col. 1, lines 13-18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Saito in view of Cook.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in

accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

- With respect to claims 4 and 21, Saito discloses a speed converter for converting the speed of packets transmitted between a plurality of first communication nodes attached to a first IEEE-1394 serial bus and a plurality of second communication nodes attached to a second IEEE-1394 serial bus, comprising:

at least one first repeater node (the multi port node is further provided with a repeater 4, fig 1; col. 3 line 28) connected to the first bus;

a first transceiver node for receiving an inbound first asynchronous packet from the first bus at a first speed via the at least one firsts repeater node and transmitting an inbound second asynchronous packet as an outbound second asynchronous packet at the first speed to the first bus via the at least one first repeater node, the first transceiver node having identifiers identifying the first transceiver node itself and the at least one first repeater node at least one second repeater node (the multi port node is further provided with a repeater 4, fig 1) connected to the second bus;

a second transceiver node for transmitting the inbound first asynchronous packet as an outbound first asynchronous packet to the second bus at a second speed via at least one second repeater node and receiving the inbound second asynchronous packet from the second bus at the second speed via the at least one second repeater node, the second transceiver node having

identifiers identifying the second transceiver node itself and the at least one second repeater node (port transceivers 10 and 11 operating with a target node over respective serial buses, are connected to a data link which performs data format conversion between the data link signals to and from port transceivers via a repeater. A first speed setting circuit located in a first port transceiver of the plurality of port transceiver and a second speed setting circuit located in a second port transceiver col. 2 lines 13-18 and col. 3 lines 7-15);

except for header translation circuitry for translating destination identifier of the inbound first asynchronous packet received by the first transceiver node to destination identifier of the outbound first asynchronous packet according to mapped relationships between the second communication nodes and the first transceiver node and the at least one first repeater node, and translating destination identifier of the inbound second asynchronous packet received by the second transceiver node to destination identifier of the outbound second asynchronous packet according to mapped relationships between the first communication nodes and the second transceiver node and the at least one second repeater node.

Cook teaches that it is known to include a system that determines if the source ID is the same as the destination ID and then through a series of processes of setting the ID's the same as set forth at col. 7 lines 53-67 and col. 8 lines 1-30. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a means of setting the source ID to the destination ID, as taught

Allowable Subject Matter

5. Claims 5-14, and 20, 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 5/17/04 have been fully considered but they are not persuasive.

- In response to Applicant's argument that Saito does not disclose or suggest the transmitting of first and second packets at first and second speed between two nodes, respectively. Examiner respectfully disagrees. These limitation is not teaching in the claim of invention.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUC H TRAN whose telephone number is (703) 308-7471. The examiner can normally be reached on M-F (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RAO SEEMA can be reached on (703) 308-5463. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phuc Tran
Assistant Examiner
Art Unit 2664

P.t
7/29/04

DANG TON
PRIMARY EXAMINER